REMARKS

This communication is responsive to the Office Action mailed April 30, 2003. Claims 1-21 remain pending in the application. Claims 19-21 are allowed. Claims 2, 6, 9, and 17 stand objected to. Claims 1, 3-5, 7-8, 10-16, and 18 stand rejected.

Section 102 Rejections

Claims 1, 3-5, 7-8, 10, 12-14, 16 and 18 stand rejected under 35 U.S.C. §102(b) as being anticipated by MacKenna et al. (U.S. Patent No. 5,319,753). Applicant respectfully traverses the rejection.

Regarding claims 1, 5, 8, and 16, the Examiner contends that MacKenna discloses an electronic system comprising: a processor; a memory having more than one memory location; and a bus connecting the processor to the memory, wherein the bus comprises: a data bus transmitting data; an address bus for identifying a first memory location; a main command bus for transmitting a first command that relates to the first memory location; and a supplementary command bus for transferring a second command wherein the second command does not relate to the first memory location. The Examiner references Column 1, lines 60-67 with respect to the supplementary command bus element.

However, MacKenna merely discloses a system for passing commands and information between two processors or devices over a traditional bus. MacKenna discloses that the commands and information are passed between the processors using interrupts. Furthermore, the commands passed over the traditional bus (main bus) are address specific commands. In particular, MacKenna column 1, lines 60-67 discloses an interrupt mechanism that facilitates the passing of interrupt vectors and associated interrupt information from one

device to another device. For example, the interrupt information is sent between processors (Col. 2, lines 22-23). MacKenna discloses that such interrupt information is written to, and read from, specific addresses (Col. 2, lines 28-39 and Col. 3, lines 35-66). The system data bus 700 and address bus 800 as disclosed in MacKenna are no different from traditional data bus structures.

In contrast, independent claims 1, 5, 8, and 16 of the present invention respectively recite, among other things, the element of "a supplementary command bus for transferring a second command, wherein the second command does not relate to the first memory location", "a supplementary command bus configured to transfer a general command", a "general command interface configured to receive only one or more general commands", and a "supplementary control interface for receiving a general command" (emphasis added).

Applicant respectfully asserts that MacKenna does not disclose a "supplementary command bus." MacKenna only discloses a traditional bus. As described in detail in the specification, a supplementary command bus functions in parallel with the traditional type of bus and is configured to carry only general (non-address specific) commands. MacKenna discloses no such supplementary command bus.

Applicant respectfully asserts that MacKenna also does not disclose a "supplementary control interface." MacKenna only discloses, if at all, a traditional control interface. As described in more detail in the specification, a supplementary control interface functions in parallel a traditional control interface. The supplementary control interface is configured to receive information from the supplementary command bus (i.e., general commands), just as the traditional control interface would receive information from a traditional bus (i.e., various information including address specific commands). Thus, because MacKenna does not

disclose a supplementary command bus, it is not surprising that MacKenna does not disclose a supplementary control interface.

General commands, as defined in the specification at page 7, paragraph 26, are commands that relate to a large block of memory locations or "that are not associated with row or column information, and thus do not use the address bus." In various ways, each of claims 1, 5, 8, and 16 involve the general (non-address specific) commands. For example, the supplementary command bus is configured to transfer general commands and the general command interface and supplementary command interface are configured to only receive general commands. Thus, Applicant respectfully asserts that MacKenna does not disclose a "supplementary command bus", a "general command interface", or a "supplementary control interface" that is dedicated to transfer/receive only general commands. For the above reasons, MacKenna does not disclose each and every element of claims 1, 5, 8, and 16, and Applicant respectfully requests allowance of these claims and the claims that depend therefrom.

Regarding claims 3-4, 7, 10, 12-14, and 18, the Examiner contends that MacKenna discloses the main command bus transfers location-specific commands, and the supplementary command bus transfers only general commands (Column 1, lines 51-65).

However, for the same reasons stated above, Applicant respectfully asserts that MacKenna does not disclose a supplementary command bus. In particular, MacKenna column 1, lines 51-65 discloses an interrupt mechanism that facilitates the passing of interrupt vectors and associated interrupt information from one device to another device. MacKenna discloses that such interrupt information is written and read from specific addresses (Col. 2, lines 28-39).

In contrast, claims 3-4 and 7 each recite a supplementary command bus configured to transfer a general (non-address specific) command. Also, claims 10, 12-14, and 18 of the present invention each recite a general command interface configured to receive a general command. MacKenna does not disclose a supplementary command bus configured to transfer a general command nor a general command interface configured to receive a general command. Therefore, MacKenna does not disclose each and every element of claims 3-4, 7, 10, 12-14, and 18, and Applicant respectfully requests allowance of these claims and the claims that depend therefrom.

Claims 11-15 stand rejected under 35 U.S.C. §102(b) as being anticipated by Nitta et al. (U.S. Patent No. 5,831,924). Applicant respectfully traverses the rejection. Regarding claims 11-15, the Examiner contends that Nitta discloses "a memory having an interface, wherein the interface comprises a general command interface configured to receive a general command."

However, Applicant respectfully asserts that Nitta discloses the internal layout of a memory array such as may be found in a SDRAM. (See Abstract, first paragraph of the Summary of the Invention, and Figure 14). Nitta discloses "one memory array" divided into a plurality of banks sharing a row of memory cells with internal buses for connecting sub arrays to the input/output buffer of the memory array. Id. Thus, Nitta discloses, if anything, a traditional command interface configured to receive data/commands and addresses for storage of that data or execution of that command.

In contrast, claim 11 recites "[a] memory having an interface, wherein the interface comprises a general command interface configured to receive a general command" (emphasis added). Nitta does not disclose a general command interface configured to receive a general

(non-address specific) command. Rather, the memory devices disclosed are configured to receive address specific commands. It is not surprising that Nitta does not disclose a memory device configured to receive general commands through a supplementary or general command interface that is configured in parallel with the traditional interface, because to do so would also involve disclosing a supplementary command bus and Nitta does not disclose anything about the command buses external to the memory device. Therefore, Applicant submits that each and every element of claim 11 is not disclosed, taught, or suggested by Nitta. Furthermore, claims 12 and 13 are not anticipated by Nitta for the additional reason that they depend from claim 11.

Regarding claim 12, the Examiner contends that Nitta additionally discloses "wherein the general command is a PRECHARGE command" (Column 18, lines 50-54). However, although Nitta does discuss the PRECHARGE function, it does not disclose receipt of the PRECHARGE command as a general command over a general command interface as recited in claim 12. In fact, Nitta does not discuss delivery of a PRECHARGE command to the device other than to discuss the typical RAS, CAS, and WE inputs through a traditional interface. Therefore, Applicant submits that each and every element of claim 12 is not disclosed, taught, or suggested by Nitta.

Regarding claim 13, the Examiner contends that Nitta discloses "wherein the memory includes more than one bank, and the interface further comprises a general bank select interface configured to receive bank address information for the general command" (Column 20, lines 60-64). However, for the reasons stated above, Nitta does not disclose the general command interface of claim 13. Thus, Applicant respectfully asserts that Nitta does not disclose a general bank select interface configured to receive bank address information for

the general command. Therefore, Applicant submits that each and every element of claim 13 is not disclosed, taught, or suggested by Nitta.

Regarding claims 14-15, the Examiner contends that Nitta discloses "a memory including a one-bit PRECHARGE input dedicated to receiving a PRECHARGE command" (Column 30, lines 42-45). However, this reference to Nitta does not disclose a one-bit PRECHARGE. Applicant respectfully asserts that Nitta discloses at least two signals for causing a PRECHARGE (i.e., RAS and CAS or WE), and moreover that the "one-bit" bus discussed at this portion of Nitta is merely an internal bus within the memory array. Thus, Nitta does not disclose a memory having a one-bit input dedicated to receiving a PRECHARGE command.

Similarly, with respect to claim 15, Applicant respectfully asserts that Nitta does not disclose a general bank select interface configured to receive bank address information for the PRECHARGE command. Therefore, Applicant submits that each and every element of claims 14 and 15 are not disclosed, taught, or suggested by Nitta.

Allowable Subject Matter

Applicant thanks the Examiner for the indication that claims 2, 6, 9, and 17 are allowable if rewritten in independent form including all of the limitation of the base claims and intervening claims. The Examiner stated that the prior art made of record does not teach or suggest the claimed limitations of claims 2, 6, 9, and 17. Claim 2 recites, in part, "wherein the second command is a PRECHARGE command." Claim 6 recites, in part, "wherein the general command is a PRECHARGE command." Claim 9 recites, in part, "wherein the general command interface is configured to receive a PRECHARGE command." Claim 17 recites, in part, "wherein the general command is a PRECHARGE command."

Applicant respectfully notes that claim 12 also includes the limitation, "wherein the general command is a PRECHARGE command." Applicant respectfully requests that claim 12 also be held allowed or allowable. Furthermore, claim 14 includes the limitation "[a] memory including a one-bit PRECHARGE input dedicated to receiving a PRECHARGE command. Applicant requests that claim 14 also be held allowed.

Applicant thanks the Examiner for allowance of claims 19-21. The Examiner stated that the prior art of record does not teach the claimed invention having a supplementary control circuit [interface] as claim 19 discloses or a method of accessing a memory as claims 20-21 disclose. Applicant notes that claims 16 and 18 also recite a supplementary control interface. Applicant requests that claims 16 and 18 also be held allowed.

B. Conclusion

Applicant respectfully submits that the present application is in condition for allowance, and earnestly solicits a Notice of Allowance at the Examiner's earliest convenience. The Examiner is invited to telephone the undersigned if such would advance prosecution of this Application in any way.

Dated this 30th day of July, 2003.

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